AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the above-identified application.

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) A charge pump circuit for use in a phase-lock loop circuit, the charge pump comprising:

a charge pump core circuit that outputs a control voltage, said charge pump core circuit including first switching elements;

a replica circuit that is coupled to the charge pump core circuit, wherein the replica circuit receives the control voltage and produces one or more bias signals that are coupled to the charge pump core circuit to minimize the difference between charge up and charge down currents generated by the charge pump core circuit and wherein said replica circuit includes second switching elements configured such that said first switching elements and said second switching elements operate with substantially identical switching characteristics.

3. (Original) The charge pump circuit of claim 2, further comprising a buffer circuit that is coupled to receive the control voltage and output the control voltage to the replica circuit.

4. (Original) The charge pump circuit of claim 3, further comprising one or more error amplifiers that are coupled to the replica circuit and the buffer circuit, the one or more error amplifiers operate to output the one or more bias signals.

5. (Original) The charge pump circuit of claim 2, further comprising:

a servo circuit coupled to the replica circuit to receive at least one bias signal; and

a driver circuit coupled between the servo circuit and the charge pump core circuit.

6. (Previously Presented) A method for operating a charge pump circuit in a phase-lock loop circuit, the method comprising:

generating an output control voltage at a charge pump core circuit;

generating one or more bias signals based on the control voltage, wherein said generating the one or more bias signals includes receiving the control voltage at a buffer circuit operative to output a version of the control voltage and using the version of the control voltage to create, at a replica circuit, the one or more bias signals; and

adjusting the operation of the core circuit based on the one or more bias signals so as to minimize a difference between charge up and charge down currents.

7. (Cancelled)

8. (Previously Presented) The method of claim 6, further comprising:

generating a current difference based on the version of the control voltage; and

generating the one or more bias signals based on the current difference.

9. (Previously Presented) A charge pump circuit for use in a phase-lock loop circuit, the charge pump circuit comprising;

a charge pump core circuit means for outputting a control voltage, said charge pump core circuit means including first switching elements; and

a replica circuit means for receiving the control voltage and producing one or more bias signals that are coupled to the charge pump core circuit means to minimize the difference between charge up and charge down currents generated by the charge pump core circuit means, said replica circuit means including second switching elements wherein substantially identical switching characteristics characterize operation of said first switching elements and said second switching elements.

10 (Original) The charge pump circuit of claim 9, further comprising a buffer circuit means for receiving the control voltage and outputting a version of the control voltage to the replica circuit means.

11 (Original) The charge pump circuit of claim 10, further comprising one or more error amplifiers means for receiving the version of the control voltage and outputting the one or more bias signals.

12 (Original) The charge pump circuit of claim 9, further comprising:

a servo circuit means for receiving the at least one bias signal; and

a driver circuit means coupled to the servo circuit means.

13 (Previously Presented) The charge pump circuit of claim 4 wherein said error amplifiers comprise transconductance amplifiers.

14 (Previously Presented) The charge pump circuit of claim 11 wherein said error amplifier means comprise transconductance amplifier means.

15 (Previously Presented) The charge pump circuit of claim 5 wherein said servo circuit is disposed to set the voltage of a driver used to switch a charge pump current.

16 (Previously Presented) The charge pump circuit of claim 12 wherein said servo circuit means is disposed to set the voltage of a driver means used to switch a charge pump current.

17 (Previously Presented) A charge pump circuit comprising;

a charge pump core circuit outputting a control voltage wherein said charge pump core circuit includes a switching circuit;

a buffer circuit coupled to said charge pump core circuit disposed to buffer said control voltage;

a replica circuit matching said charge pump core circuit for receiving the buffered control voltage and producing one or more bias signals; and

a transconductance amplifier for generating a signal to minimize the difference between charge up and charge down currents generated by the charge pump core circuit.

18 (Previously Presented) The charge pump circuit of claim 17 further comprising a switch driver disposed to control a current switch.

19 (Previously Presented) The charge pump circuit of claim 18 wherein said switch driver comprises a field effect transistor.

20 (Previously Presented) The charge pump circuit of claim 18 wherein said switch driver comprises a bipolar junction transistor.

21 (Cancelled)